74HC163; 74HCT163

Presettable synchronous 4-bit binary counter; synchronous reset

Rev. 3 — 2 June 2014 Product data sheet

1. General description

The 74HC163; 74HCT163 is a synchronous presettable binary counter with an internal look-head carry. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP). The outputs (Q0 to Q3) of the counters may be preset to a HIGH or LOW. A LOW at the parallel enable input ($\overline{PE}$) disables the counting action. It causes the data at the data inputs (D0 to D3) to be loaded into the counter on the positive-going edge of the clock. Preset takes place regardless of the levels at count enable inputs (CEP and CET). A LOW at the master reset input ($\overline{MR}$) sets Q0 to Q3 LOW after the next positive-going transition on the clock input (CP). This action occurs regardless of the levels at input pins $\overline{PE}$, CET and CEP. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate. The look-ahead carry simplifies serial cascading of the counters. Both CEP and CET must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH output of Q0. This pulse can be used to enable the next cascaded stage. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

The CP to TC propagation delay and CEP to CP set-up time determine the maximum clock frequency for the cascaded counters according to the following formula:

$$f_{max} = \frac{1}{t_{P(max)}(CPtoTC) + t_{SU}(CEPtoCP)}$$

2. Features and benefits

- Complies with JEDEC standard no. 7A
- Input levels:
  - For 74HC163: CMOS level
  - For 74HCT163: TTL level
- Synchronous counting and loading
- 2 count enable inputs for n-bit cascading
- Synchronous reset
- Positive-edge triggered clock
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from −40 °C to +85 °C and −40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC163N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HCT163N				
74HC163D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT163D				
74HC163DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT163DB				
74HC163PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT163PW				

4. Functional diagram

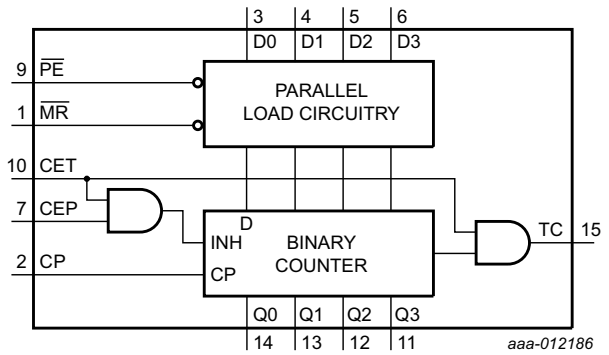


Fig 1. Functional diagram

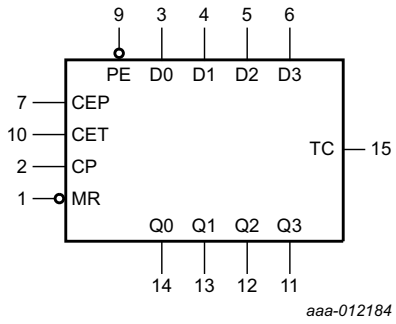


Fig 2. Logic symbol

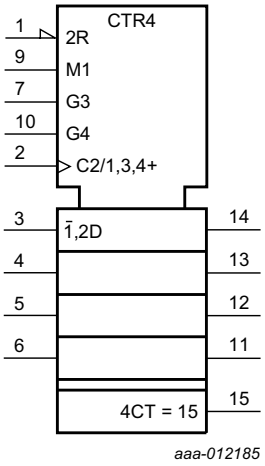


Fig 3. IEC logic symbol

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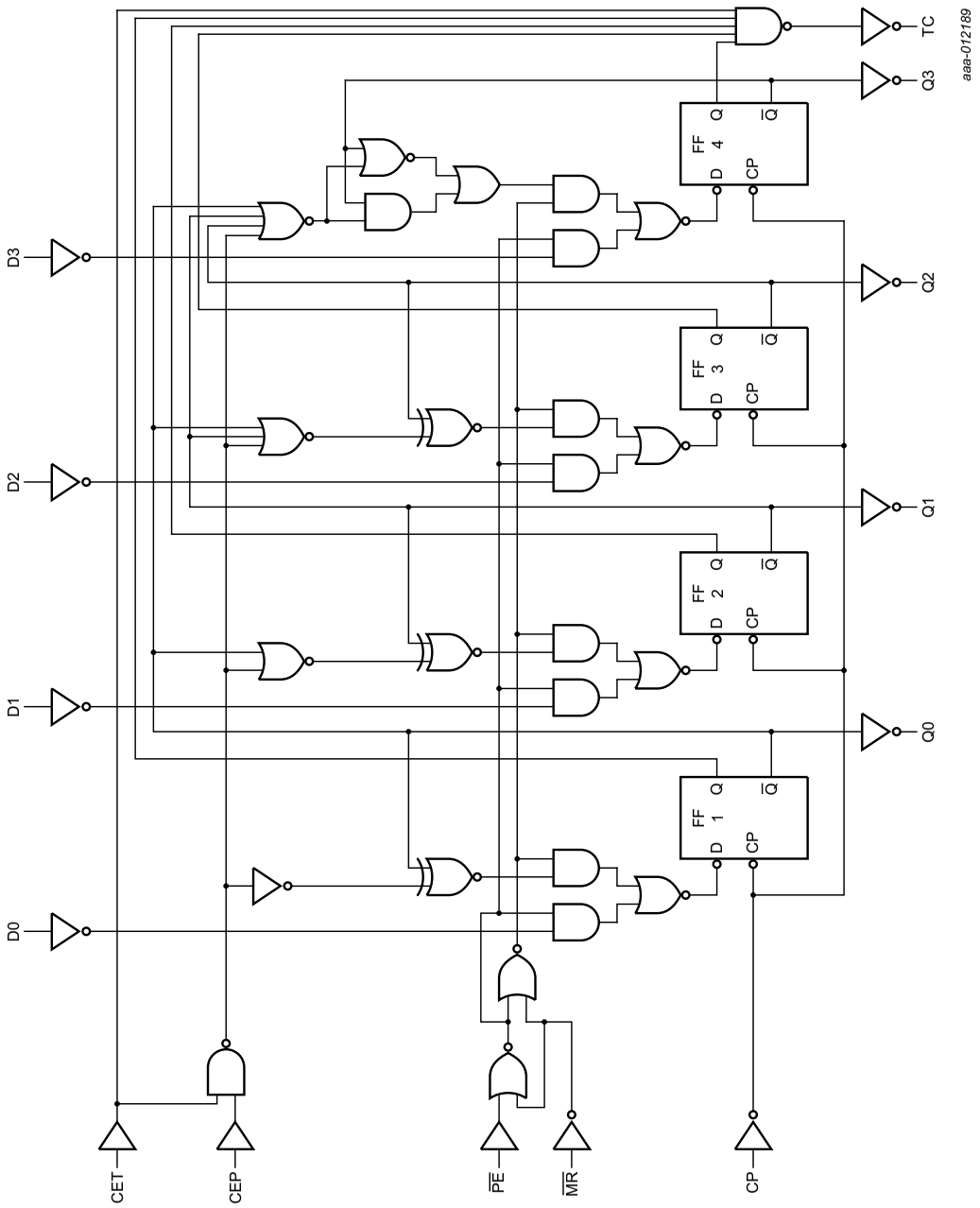


Fig 4. Logic diagram

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5. Pinning information

5.1 Pinning

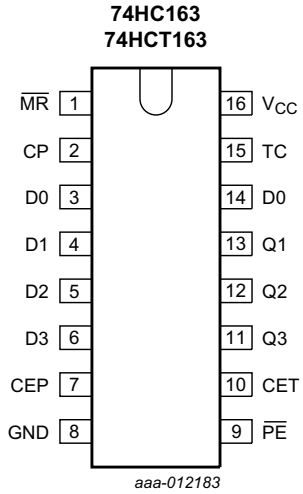


Fig 5. Pin configuration DIP16

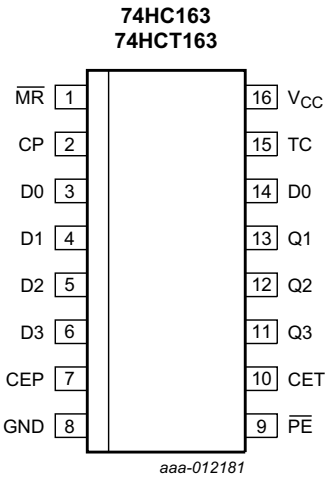


Fig 6. Pin configuration SO16

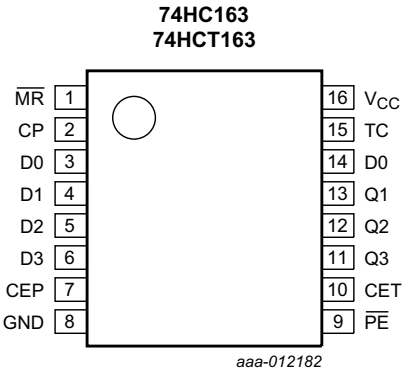


Fig 7. Pin configuration TSSOP16 and SSOP16

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{MR}$	1	synchronous master reset (active LOW)
CP	2	clock input (LOW-to-HIGH, edge triggered)
D0, D1, D2, D3	3, 4, 5, 6	data input
CEP	7	count enable input
GND	8	ground (0 V)
$\overline{PE}$	9	parallel enable input (active LOW)
CET	10	count enable carry input
Q0, Q1, Q2, Q3	14, 13, 12, 11	flip-flop output
TC	15	terminal count output
V_{CC}	16	supply voltage

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6. Functional description

Table 3. Function table[1]

Operating mode	Inputs						Outputs	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	Dn	Qn	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	L
Count	h	↑	h	h	h	X	count	
Hold (do nothing)	h	X	l	X	h	X	qn	L
	h	X	X	l	h	X	qn	L

[1] The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH);
H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition;
X = don't care;
↑ = LOW-to-HIGH clock transition.

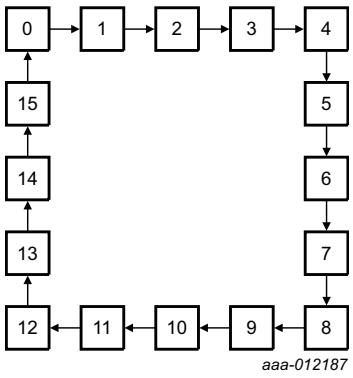
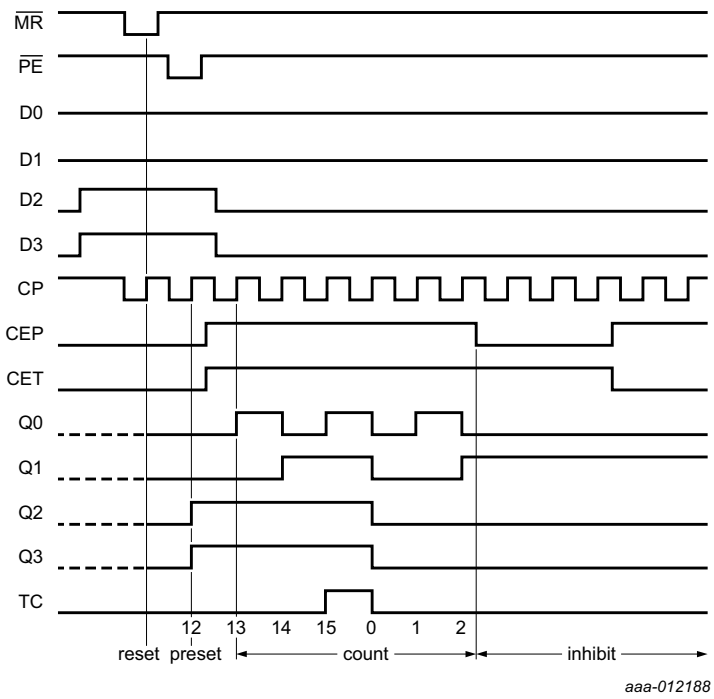


Fig 8. State diagram

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Sequence

reset outputs to zero; preset to binary 12; count to 13, 14, 15, zero, one and two; inhibit.

Fig 9. Typical timing sequence

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		−50	-	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	DIP16 package [1]	-	750	mW
		SO16 package [1]	-	500	mW
		(T)SSOP16 package [1]	-	500	mW

[1] For DIP16 packages: above 70 °C the value of P_{tot} derates linearly at 12 mW/K.
For SO16 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.
For (T)SSOP16 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.

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8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC163			74HCT163			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		−40	+25	+125	−40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC163										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = −20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = −20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = −4.0; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = −5.2; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80.0	-	160.0	μA

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Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT163										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = −20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = −4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	-	80.0	-	160.0	μA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} − 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A								
		pin $\overline{MR}$	-	95	342	-	427.5	-	465.5	μA
		pin CP	-	110	396	-	495	-	539	μA
		pin CEP and Dn	-	25	90	-	112.5	-	122.5	μA
		pin CET	-	75	270	-	337.5	-	367.5	μA
		pin $\overline{PE}$	-	30	108	-	135	-	147	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

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10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 15.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC163										
t_{pd}	propagation delay	CP to Qn; see Figure 10 [1]	-							
		V_{CC} = 2.0 V	-	55	185	-	230	-	280	ns
		V_{CC} = 4.5 V	-	20	37	-	46	-	56	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	17	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	16	31	-	39	-	48	ns
		CP to TC; see Figure 10								
		V_{CC} = 2.0 V	-	69	215	-	270	-	320	ns
		V_{CC} = 4.5 V	-	25	43	-	54	-	65	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	21	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	20	37	-	46	-	55	ns
		CET to TC; see Figure 11								
		V_{CC} = 2.0 V	-	36	120	-	150	-	180	ns
		V_{CC} = 4.5 V	-	13	24	-	30	-	36	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	11	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	10	20	-	26	-	31	ns
t_t	transition time	see Figure 10 and Figure 11 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_W	pulse width	CP; HIGH or LOW; see Figure 10								
		V_{CC} = 2.0 V	80	17	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	6	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	5	-	17	-	20	-	ns

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Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 15.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{su}	set-up time	$\overline{MR}$, Dn to CP; see Figure 12 and Figure 13								
		V_{CC} = 2.0 V	80	17	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	6	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	5	-	17	-	20	-	ns
		$\overline{PE}$ to CP; see Figure 12								
		V_{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20	-	ns
		CEP, CET to CP; see Figure 14								
		V_{CC} = 2.0 V	175	58	-	220	-	265	-	ns
		V_{CC} = 4.5 V	35	21	-	44	-	53	-	ns
		V_{CC} = 6.0 V	30	17	-	37	-	45	-	ns
t_h	hold time	Dn, $\overline{PE}$, CEP, CET, $\overline{MR}$ to CP; see Figure 12, Figure 13 and Figure 14								
		V_{CC} = 2.0 V	0	–14	-	0	-	0	-	ns
		V_{CC} = 4.5 V	0	–5	-	0	-	0	-	ns
		V_{CC} = 6.0 V	0	–4	-	0		0	-	ns
f_{max}	maximum frequency	CP; see Figure 10								
		V_{CC} = 2.0 V	5	15	-	4	-	4	-	MHz
		V_{CC} = 4.5 V	27	46	-	22	-	18	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	51	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	32	55	-	26	-	21	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 5 V; f_i = 1 MHz [3]	-	33	-	-	-	-	-	pF

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Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 15.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT193										
t_{pd}	propagation delay	CP to Qn; see Figure 10 [1]								
		V_{CC} = 4.5 V	-	23	39	-	49	-	59	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	20	-	-	-	-	-	ns
		CP to TC; see Figure 10								
		V_{CC} = 4.5 V	-	29	49	-	61	-	74	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	25	-	-	-	-	-	ns
		CET to TC; see Figure 11								
		V_{CC} = 4.5 V	-	17	32	-	44	-	48	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	14	-	-	-	-	-	ns
t_t	transition time	see Figure 10 and Figure 11 [2]								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t_W	pulse width	CP; HIGH or LOW; see Figure 10								
		V_{CC} = 4.5 V	20	6	-	25	-	30	-	ns
t_{su}	set-up time	$\overline{MR}$, Dn to CP; see Figure 12 and Figure 13								
		V_{CC} = 4.5 V	20	9	-	25	-	30	-	ns
		$\overline{PE}$ to CP; see Figure 12								
		V_{CC} = 4.5 V	20	11	-	25	-	30	-	ns
		CEP, CET to CP; see Figure 14								
		V_{CC} = 4.5 V	40	24	-	50	-	60	-	ns
t_h	hold time	Dn, $\overline{PE}$, CEP, CET, $\overline{MR}$ to CP; see Figure 12, Figure 13 and Figure 14								
		V_{CC} = 4.5 V	0	–5	-	0	-	0	-	ns
f_{max}	maximum frequency	CP; see Figure 10								
		V_{CC} = 4.5 V	26	45	-	21	-	17	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	50	-	-	-	-	-	MHz

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Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 15.

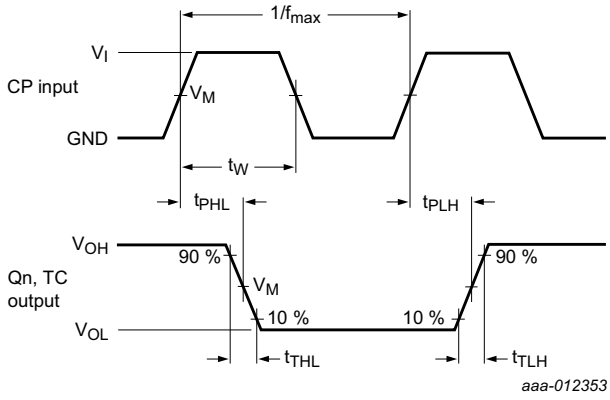
Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} − 1.5 V; V_{CC} = 5 V; f_i = 1 MHz [3]	-	35	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms



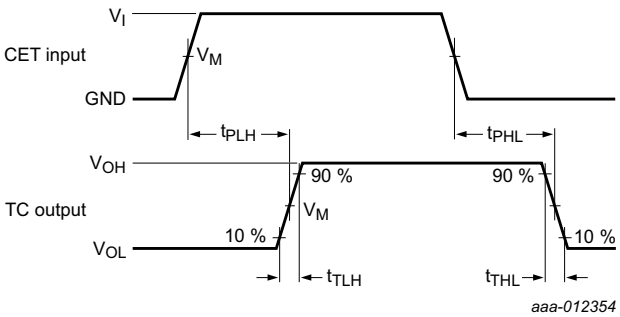
Measurement points are given in Table 8.

Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 10. The clock (CP) to outputs (Qn, TC) propagation delays, pulse width, output transition times and maximum frequency

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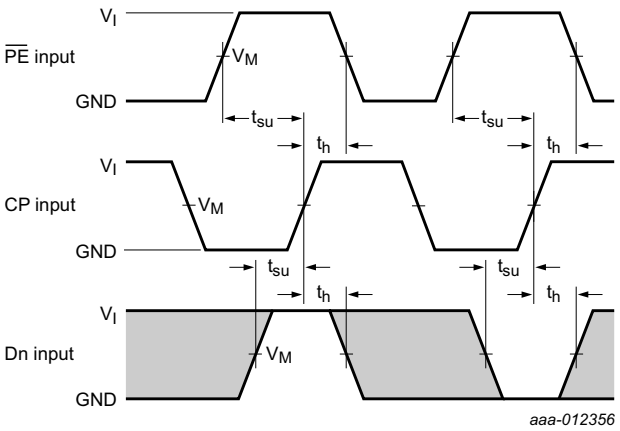
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Measurement points are given in Table 8.

Logic levels V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 11. The count enable carry input (CET) to terminal count output (TC) propagation delays and output transition times



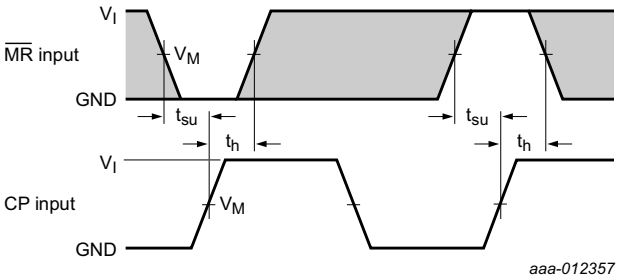
The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in Table 8.

Fig 12. The data input (Dn) and parallel enable input ($\overline{PE}$) set-up and hold times

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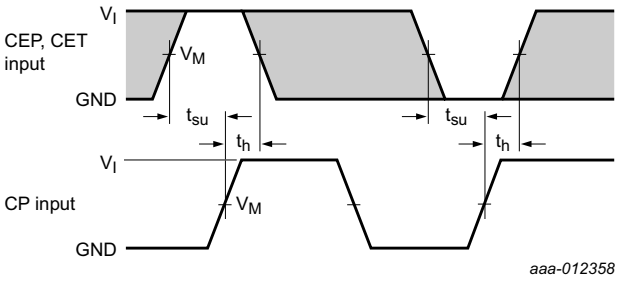
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The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in Table 8.

Fig 13. The master reset ($\overline{MR}$) set-up and hold times



The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in Table 8.

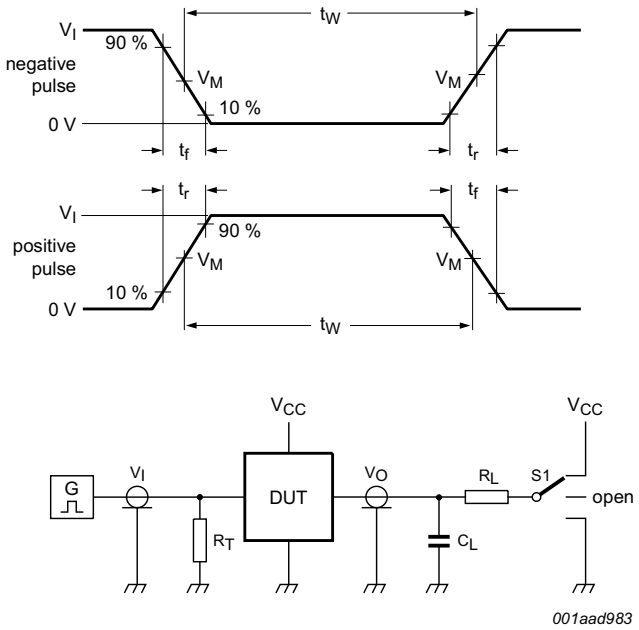
Fig 14. The count enable input (CEP) and count enable carry input (CET) set-up and hold times

Table 8. Measurement points

Type	Input		Output
	V_M	V_I	V_M
74HC163	$0.5 \times V_{CC}$	GND to V_{CC}	$0.5 \times V_{CC}$
74HCT163	1.3 V	GND to 3 V	1.3 V

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Test data is given in Table 9.

Test circuit definitions:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

R_L = Load resistance.

S1 = Test selection switch

Fig 15. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC163	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open
74HCT163	3 V	6 ns	15 pF, 50 pF	1 kΩ	open

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12. Application information

The 74HC163; 74HCT63 facilitate designing counters of any modulus with minimal external logic. The output is glitch-free due to the synchronous reset.

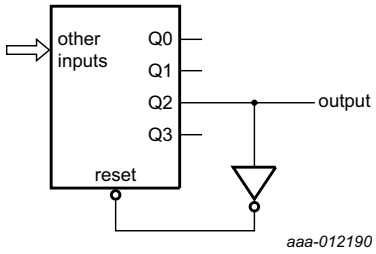


Fig 16. Modulo-5 counter

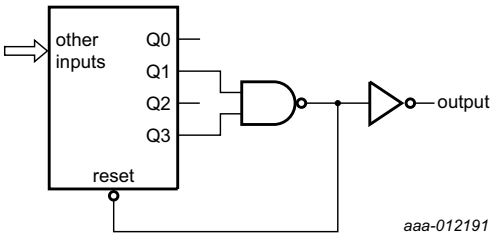


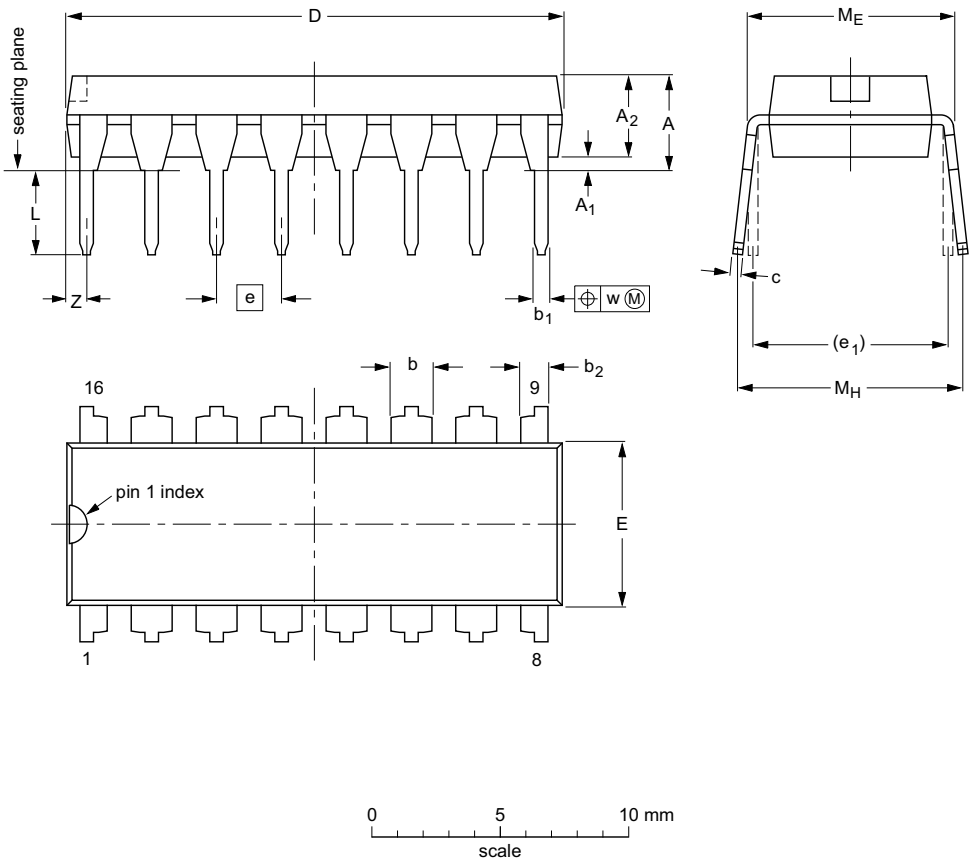
Fig 17. Modulo-11 counter

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13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

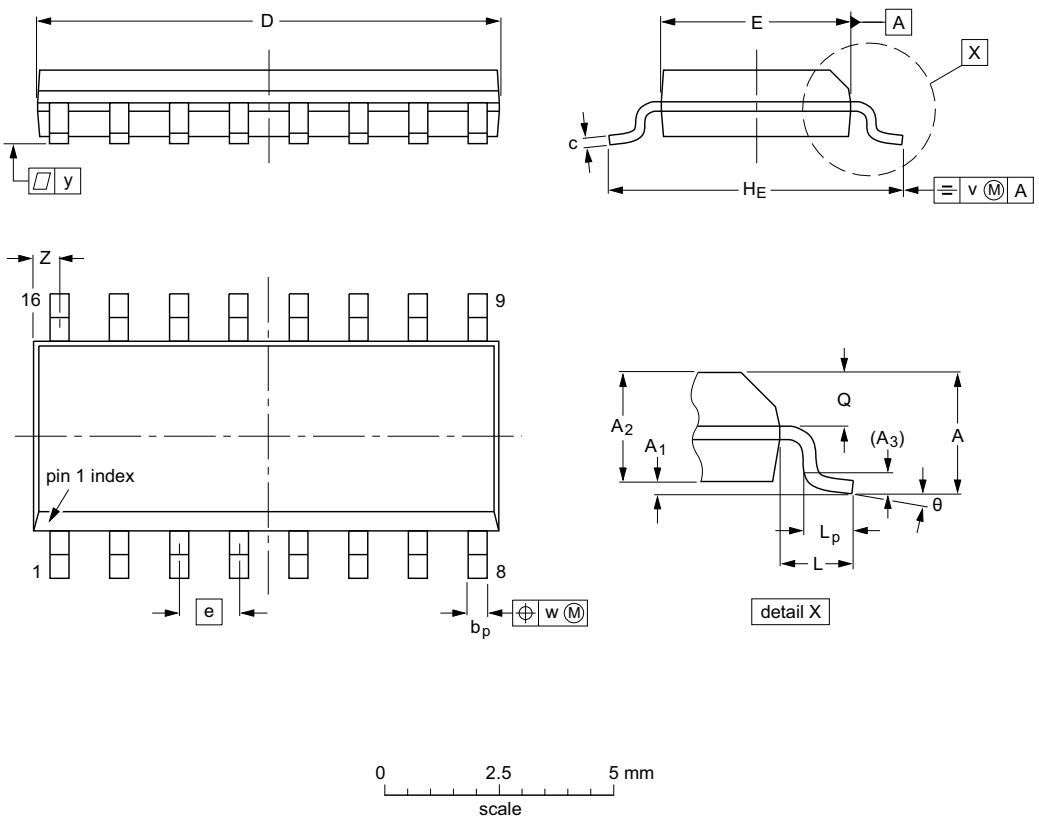
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 18. Package outline SOT38-4 (DIP16)

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SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

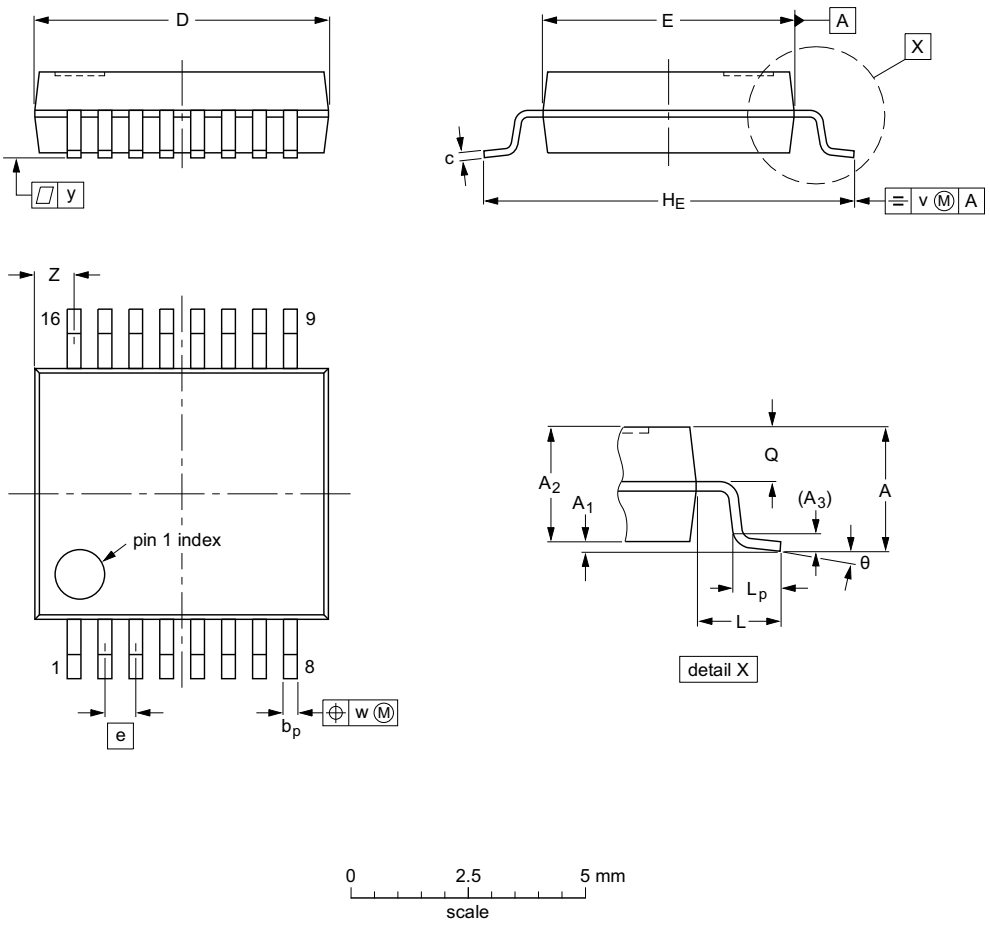
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SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 19. Package outline SOT109-1 (SO16)

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SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

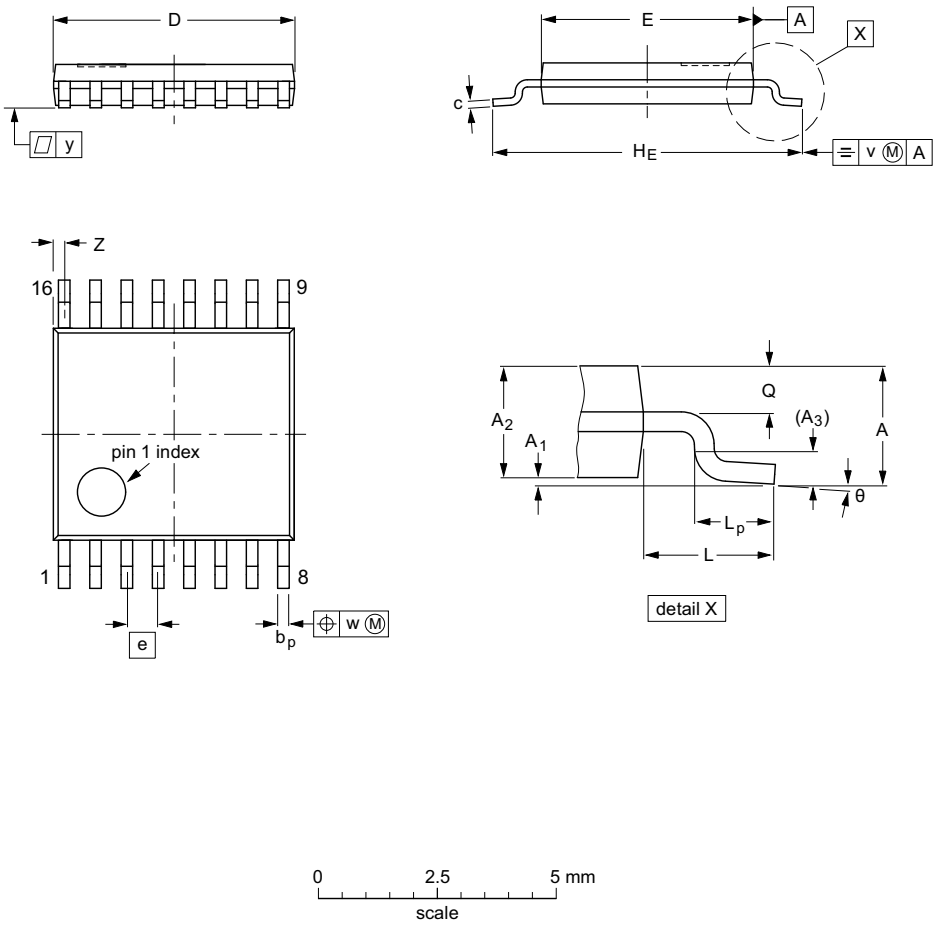
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 20. Package outline SOT338-1 (SSOP16)

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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 21. Package outline SOT403-1 (TSSOP16)

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14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT163 v.3	20140602	Product data sheet	-	74HC_HCT163_CNV v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT163_CNV v.2	19930927	Product specification	-	-

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16. Legal information

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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